Nanowire field-effect transistor with $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ dielectric

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Nanowire field-effect transistor with $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ dielectric

Wangyang Fu, Zhi Xu, Kaihui Liu, Wenlong Wang, Xuedong Bai,[a),b)] and Enge Wang[a),c)]
Beijing National Laboratory for Condensed Matter Physics, Institute of Physics, Chinese Academy of Sciences, Beijing 100190, China

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In this letter, amorphous $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ films with large permittivity (~70) are prepared as the gate dielectric for ZnO nanowire field-effect transistors by using low-temperature (~100 °C) pulsed laser deposition. The transistors exhibit a low operation gate voltage (<3 V), a high carrier mobility (~42 cm^2/V s), and a steep subthreshold swing up to 240 mV/decade. These results combined with near-room-temperature processing technique suggest that the nanowire transistor with $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ dielectric is a promising candidate for high-performance flexible electronics. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3037219]

Low-cost, large-area, and flexible electronics[1,2] are attractive for their wide applications as electronic paper, transparent and flexible display, etc. In these technologies, low-temperature processing is critical for the use of flexible polymer substrates. The newly emerging organic thin-film transistors (TFTs), although compatible with low-temperature processing, suffer from their relatively low carrier mobility which leads to poor device performances, such as high power consumption and long display response time. Recently, the inorganic semiconductor nanowire (NW) transistors have been intensively investigated for their fundamental advantages of high carrier mobility and low-temperature compatibility.[3–11] It is well documented that high-κ thin dielectric films, which ensure the increased coupling between the gate electrode and NW channel, are crucial for the fabrication of high-performance NW transistor devices. However, in most cases, the deposition of high-κ dielectric was carried out at high temperature, which is not compatible with flexible polymer substrates. In addition, it is also observed that thin gate dielectric (~10 nm) deposited on rough flexible polymer substrates is susceptible to pinhole formation, which would lead to poorer performance and low manufacturing yields of the devices. Therefore, the exploration of low-temperature processing and large-permittivity dielectric of NW transistors, which affords high capacitance without relying on very thin films, is highly desirable.

Pyrochlore $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ (BZN),[12–16] which exhibits the highest permittivity (~70) until now for dielectric films prepared by room-temperature deposition, provides us an ideal gate dielectric. ZnO TFTs and organic TFTs (OTFTs) with amorphous BZN dielectric have been fabricated at room temperature,[17,18] but their effective carrier mobilities are still quite low (<0.5 cm^2/V s).

In this letter, we report on the gate processing to fabricate ZnO NW field-effect transistors (FETs) at low temperature by using BZN as dielectric, which is suitable for flexible electronic applications. Compared with the conventional OTFTs, the BZN-gated ZnO NW transistor offers significantly higher carrier mobility (~42 cm^2/V s), which is a significant step in achieving high-performance flexible electronics.

The single-crystalline ZnO NWs were grown by the thermal evaporation method.[19] ZnO NWs were dispersed in ethanol and then spin-coated onto a heavily doped *n*-type silicon substrate with 100 nm thick silicon dioxide layer, following which 200 nm thick BZN film was deposited in 10 Pa of O_2 environment at 100 °C by using pulsed laser deposition. The x-ray diffraction (XRD) pattern, shown in Fig. 1(a), indicates the amorphous structure of BZN films. The FETs are based on an integration of individual NWs and amorphous BZN dielectric. A representative atomic force microscopy (AFM) image of the as-deposited BZN film on SiO_2/Si substrate is shown in Fig. 1(a) inset, which depicts a surface morphology with average grain size of around 30 nm and root-mean-square roughness of ~1.5 nm. The condensed and smooth film would ensure a high-quality ZnO/BZN interface that is useful for high-performance FET devices. In

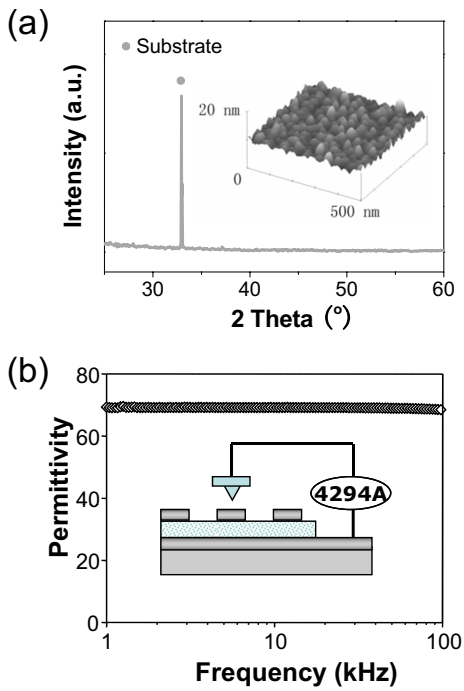

FIG. 1. (Color online) Characteristics of BZN dielectric layer. (a) XRD pattern of the BZN film and AFM image of the as-deposited BZN film (inset). (b) Permittivity as a function of frequency for the amorphous BZN film, measured without dc bias field. Inset is the Pt/BZN/Pt/SiO_2/Si paralleled structure for capacitance measurement.

[a)]Authors to whom correspondence should be addressed.
[b)]Electronic mail: xdbai@aphy.iphy.ac.cn.
[c)]Electronic mail: egwang@aphy.iphy.ac.cn.

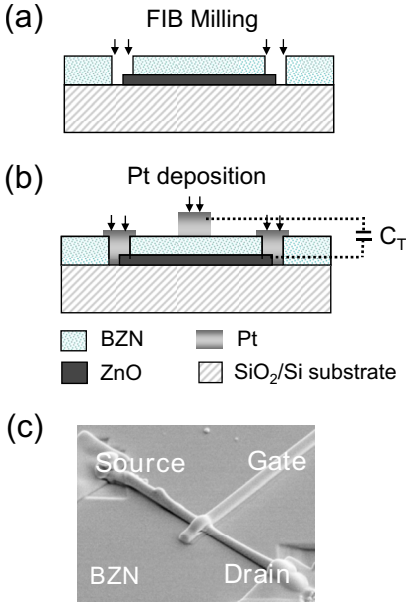

FIG. 2. (Color online) Scheme of the fabrication processing for top-gated ZnO NW FET with BZN dielectric. (a) Ion beam was focused at both ends of the individual ZnO NW to mill away the BZN layers and uncover the clean ZnO NW surface. (b) Pt is deposited onto both ends of the exposed ZnO NW and across the middle of the ZnO NW, thus forming the source, drain, and gate electrodes. (c) SEM image of the fabricated top-gated ZnO NWT with BZN dielectric.

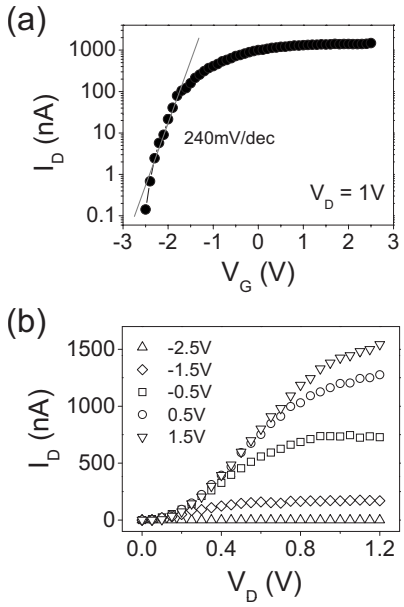

FIG. 3. Electric transport measurements. (a) I-V_G transfer characteristics of the ZnO NW FET with BZN top gate. (b) Curves of current vs source-drain bias under various gate voltages.

order to characterize the dielectric properties of the BZN films, the same deposition process was applied to prepare amorphous BZN films on $Pt/SiO_2/Si$ substrates, followed by the deposition of 100 nm thick Pt top electrode to construct a $Pt/BZN/Pt/SiO_2/Si$ paralleled capacitance. Figure 1(b) presents the frequency dependent permittivity of the amorphous BZN film measured at room temperature without the dc bias field (by using instrument Agilent 4294A). The frequency-independent permittivity of the BZN film in the range between 1 and 100 kHz is basically consistent with previous literatures.[17,18]

For device fabrication, focus ion beam (FIB) sputter milling and Pt deposition assisting were applied, as schematically illustrated in Fig. 2. First, ion beam was focused at both ends of the selected individual ZnO NW to mill away the BZN layers and uncover the clean ZnO NW surface for good electrical contact [Fig. 2(a)]. We then applied FIB assisted Pt deposition to prepare 100 nm thick Pt films on both ends of the exposed ZnO NW and also across the middle of the BZN-covered ZnO NW to form source, drain, and gate electrodes, respectively [Fig. 2(b)]. By this processing, up to five Pt top-gated ZnO NW transistors with BZN dielectric were fabricated. A typical scanning electron microscope (SEM) image of the fabricated top-gated ZnO NW FET is shown in Fig. 2(c).

The measured I-V_G transfer characteristics of the prototype NW transistor is displayed in Fig. 3(a). The device acts as a n-type Schottky-barrier transistor and exhibits a I_{on}/I_{off} ratio of 10^4 within a gate voltage of 3 V. The gate leakage current through the BZN insulator is negligible in the whole gate voltage sweeping range ($<10^{-12}$ A). Taking the geometry of the top-gated device into account, a leakage current density of less than 1 mA/cm^2 is estimated within an electric bias field of ± 150 kV/cm, which is consistent with the previous literature (~ 1 uA/cm^2 at 100 kV/cm).[18] The subthreshold swing $S=dV_G/d(\log I_D)$ is another key transistor parameter for low threshold voltage and low power operation. Here, we can deduce a $S\sim 240$ mV/decade for the prototype top-gated transistor, which is comparable with that of the state-of-the-art NW FETs (~ 200 mV/decade).[3–11] Figure 3(b) shows the current versus source-drain bias voltage curves of the NW FET under various gate voltages, whose shapes resemble those of conventional n-MOSFETs but with a Schottky barrier. A transconductance of $g_m=550$ nA/V can be deduced from the saturation regions of the curves.

In order to obtain the efficient carrier mobility of the device, we simulated the electrostatic gate-coupling

TABLE I. Comparison between the transistor characteristics of the prototype ZnO NW FET with BZN dielectric and those of previously reported high-performance NW FETs or OTFTs.

	On-current (μA)	Operng voltage (V)	Subthreshold swing (mV/decade)	Carrier mobility ($cm^2/V\,s$)	Gate dielectric
ZnO[a]	2	3	300	70	15 nm-SAS (3)
In_2O_3[a]	10	4	160	300	18 nm-Al_2O_3 (9)
OTFT[b]	1	5	300	0.5	200 nm-BZN (70)
ZnO	1.5	3	240	42	200 nm-BZN (70)

[a]Reference 4.
[b]Reference 18.

capacitance per unit length between the ZnO NW and the top Pt gate: $C_T = 1.3 \times 10^{-9}$ F/m, by using the partial differential equation method (BZN permittivity $\varepsilon = 70$, $h = 200$ nm, and NW radius $r = 50$ nm). As a result, the electron mobility of the device can be estimated as $u = g_m L / V_D C_T = 42$ cm^2/V s by using the standard transistor mode, where L/V_D is taken proportionally as 10 μm/1 V.

Table I shows a comparison between the transistor characteristics of our prototype ZnO NW FET with BZN dielectric and those of previously reported high-performance NW FETs or OTFTs. Our experimental data are listed in the bottom row. It is noteworthy that the carrier mobility of our ZnO NW transistors with BZN dielectric is significantly higher than those of the recently developed OTFT (0.5 cm^2/V s) (Ref. 18) and the other parameters of our prototype device are comparable with those of the state-of-the-art NW transistors. In the present study, a thick BZN layer was applied in order to ensure manufacturing yields and lower gate leakage current. With reduction in the dielectric layer thickness, much higher performances are expected.

An important issue for integrating BZN dielectric is that it is chemically benign to the conduction channel. This is confirmed in our systematic experiments, which reveal that the mobility of ~42 cm^2/V s of the top-gated NWTs is higher than those (several to tens of cm^2/V s) of ZnO NWTs without BZN covering.

In summary, we have fabricated ZnO NW FETs by using amorphous BZN as gate insulator via a near room-temperature processing route. The high performance of NW FETs, i.e., a low operating gate voltage <3 V, a high carrier mobility ~42 cm^2/V s, and a steep subthreshold swing up to 240 mV/decade, is achieved by integration of high-permittivity dielectric and low-temperature processing, which suggests that the NW FET with BZN dielectric is a promising candidate for future flexible electronics.

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